What is claimed is:

[Claim 1] 1. A structure comprising:

a substrate;

a buried isolation layer over said substrate;

a fin field effect transistor (FinFET) over said buried isolation layer; and

a field effect transistor (FET) in said substrate, wherein a gate region of said FET is planar to a gate region of said FinFET.

[Claim 2] 2. The structure of claim 1, further comprising retrograde well regions in said substrate.

[Claim 3] 3. The structure of claim 1, wherein said FinFET comprises:

a semiconductor layer comprising sidewalls;

a first dielectric layer over said semiconductor layer;

a second dielectric layer along each of said sidewalls of said semiconductor layer;

the FinFET gate region over the first and second dielectric layers; and

FinFET source/drain regions on opposite sides of said FinFET gate region.

[Claim 4] 4. The structure of claim 1, wherein said FET comprises:

FET source/drain regions on opposite sides of the FET gate region; and

a gate dielectric layer between said FET gate region and said substrate.

[Claim 5] 5. The structure of claim 1, further comprising a shallow trench isolation region in said substrate.

[Claim 6] 6. A structure comprising:

a silicon-on-insulator (SOI) wafer comprising:

a substrate;

a buried insulator layer over said substrate; and
a semiconductor layer over said buried insulator layer;

a fin field effect transistor (FinFET) over said buried insulator layer; and

a field effect transistor (FET) integrated in said substrate, wherein a gate region of said FET is planar to a gate region of said FinFET.

[Claim 7] 7. The structure of claim 6, further comprising retrograde well regions in said substrate.

[Claim 8] 8. The structure of claim 6, wherein said FinFET comprises:

sidewalls on said semiconductor layer;
a first FinFET dielectric layer over said semiconductor layer;
a second FinFET dielectric layer along each of said sidewalls of said semiconductor layer;
the FinFET gate region over the first and second FinFET dielectric layers; and
FinFET source/drain regions on opposite sides of said FinFET gate region.

[Claim 9] 9. The structure of claim 6, wherein said FET comprises:

FET source/drain regions on opposite sides of the FET gate region; and

a gate dielectric layer between said FET gate region and said substrate.

[Claim 10] 10. The structure of claim 6, wherein said buried insulator layer comprises buried oxide.

[Claim 11] 11. The structure of claim 6, further comprising a shallow trench isolation region in said substrate.

[Claim 12] 12. A method of forming a planar substrate device integrated with a fin field effect transistor (FinFET), said method comprising:

providing a substrate;

forming a buried isolation layer above said substrate;
bonding a semiconductor layer to said buried isolation layer;
simultaneously forming a FinFET over said buried isolation layer, said FinFET comprising a FinFET gate region, and forming a field effect transistor (FET) in said substrate, said FET comprising a FET gate region; and
planarizing said FinFET gate region and said FET gate region.

[Claim 13] 13. The method of claim 12, further comprising configuring well regions in said substrate.

[Claim 14] 14. The method of claim 12, wherein said forming of said FinFET comprises:

forming a first FinFET dielectric layer over said semiconductor layer, wherein said semiconductor layer comprises sidewalls;
configuring a second FinFET dielectric layer along each of said sidewalls of said semiconductor layer and over said substrate;
forming said FinFET gate region over the first and second FinFET dielectric layers; and
forming FinFET source/drain regions on opposite sides of said FinFET gate region.

[Claim 15] 15. The method of claim 12, wherein said forming of said FET comprises:

forming a FET gate dielectric layer over said substrate;
forming said FET gate region over said FET gate dielectric layer, wherein said FET gate dielectric layer is adjacent to said FET gate region; and
forming FET source/drain regions in said substrate.

[Claim 16] 16. The method of claim 15, wherein said FET gate dielectric layer is formed between said FET gate region and said substrate.

[Claim 17] 17. The method of claim 12, further comprising configuring a shallow trench isolation region in said substrate.

[Claim 18] 18. The method of claim 12, wherein said FinFET gate region is formed of polysilicon.

[Claim 19] 19. The method of claim 12, wherein said FET gate region is formed of polysilicon.

[Claim 20] 20. The method of claim 12, wherein said buried insulator layer is formed of buried oxide.